



A Systematic Approach to Reduce Wirebond defects caused by Tight Wire Loop Profile on Ball Grid Array Packages

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read and approved the final manuscript.

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ABSTRACT

Wirebond quality aspects on a semiconductor manufacturing is one of the key factors to be considered in having a robust product. Certain criteria are defined, met, and affects the output on the product. Other variables from downstream process are also taken in account to affect the response, specific die position or placement on die attach is one example. Without controlling this input factor, unwanted out of specification response will occur and may result to rejections on the next process. This paper will focus on how to address the wire tight loop on wire bond process by analyzing the problem through systematic approach using statistical tools improving the current performance of die placement on BGA products.

Keywords: *Integrated circuit; wire bond process; die attach process; wire loop; ball grid array; semiconductor; die placement.*

1. INTRODUCTION

Continuous improvement on every manufacturing business has always been the key to a successful supplier-customer relationship. The

dedication of every individual in a large workplace to achieve a safe, innovative, quality products and outstanding services plays a big role in the world of industry. In the semiconductor industry, wherein integrated circuits (IC) are

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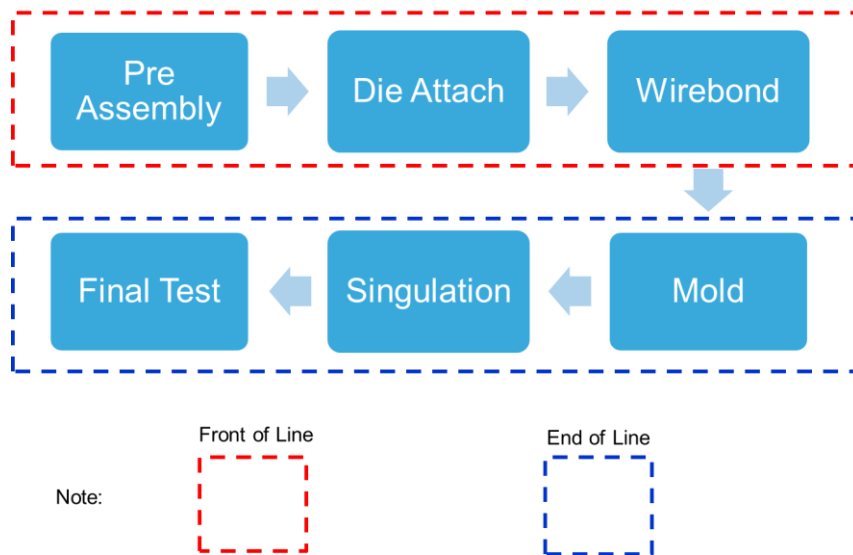


Fig. 1. Ball Grid Array (BGA) Package Process Flow

produced and assembled, technical and management trainings are offered to improve the quality of problem solving and assessing risk for both customer and supplier. Six sigma approach are one of the disciplines as discussed on [1-4] proven to effectively addresses sporadic and chronic issues, resulted to a robust, effective, and efficient solution that do not compromise yet improve the quality of end products. One literature on [5] discussed about the improvement done on the same package having a defect of silhouette die in semiconductor industry [6,7]. One of six sigma techniques like DOE or design of experiments were performed using different number of evaluations called legs and come up with a resolution to address the problem.

Our organization, together with my colleagues on the semiconductor field of manufacturing will be discussing on this manuscript one of the phenomena encountered by the production line during assembly of integrated circuits.

Challenges on every process of BGA or Ball Grid Array semiconductor package are not new and always anticipated, on every process of Front of Line (FOL) and End of Line (EOL). Fig. 1 shows the simplified process flow of the product from front to end of line. Starting with the FOL wherein sensitive parts of the integrated circuits such as substrate and silicon wafer, are singulated to become a die/dice. It will be then picked and assembled on die attach process and connected by gold wire through wire bonding process. To complete the assembly, wire bonded units on the

substrate will be covered by resin on mold process. Molded units will be subject to curing and clearing out of excess mold parts via chemical or mechanical [8,9]. Then it will be cut and singulated individually using a singulation machine. Final step of inspection will be performed, and assembled parts will be tested prior sending to customer to ensure quality of products.

2. METHODOLOGY

The focus of this paper will be on the processes affecting quality of the interconnection between die and substrate. This will include Die attach and wire bond processes. Using die attach machine with bond head, it will pick and attach singulated dice from the silicon wafer using epoxy adhesive. Consistent die position or die placement is set up and defined as it will be one of the factors of a good wire bonding. After oven curing of the epoxy, it will be connected using gold wires to have an electrical connection and functions to its desired output. Certain parameters are also defined on a Wirebond machine to have a desirable wire loop profile from the die to the leads of the substrate or vice versa. Looping profile as mentioned on [10,11] is automatically computed by the machine including its angle, kink, and wire span making it fully optimized wire bonding process. Fig. 2. Shows how die attach process is performed using singulated die and die attach material, and Fig. 3 shows how wire bond process works interconnecting the die with gold wires.

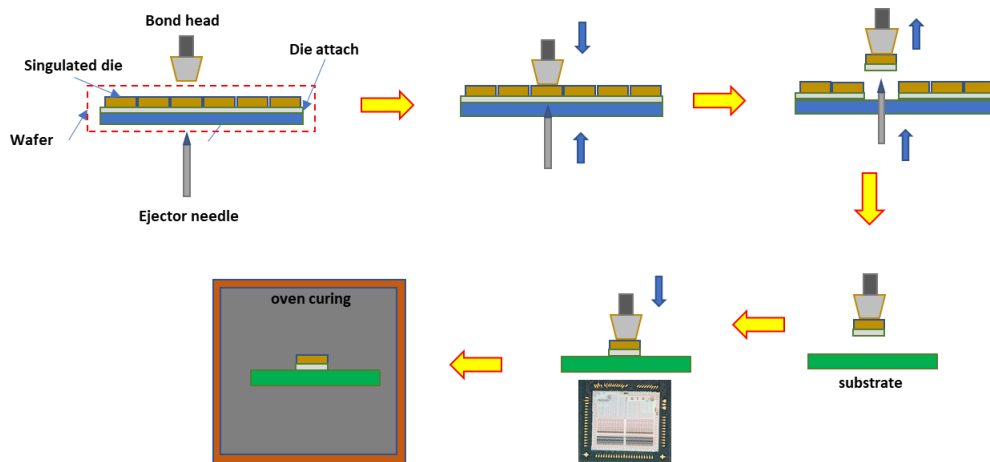


Fig. 2. Die attach process of BGA package

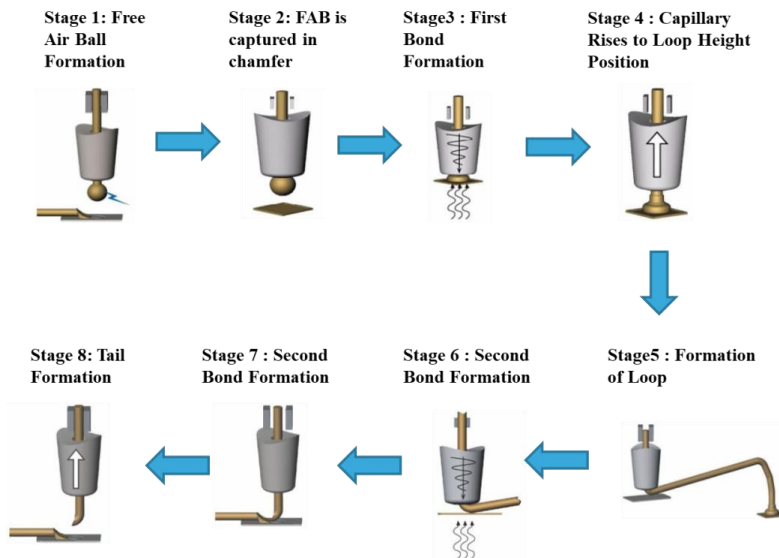


Fig. 3. Wire bonding process on BGA packages using gold wire

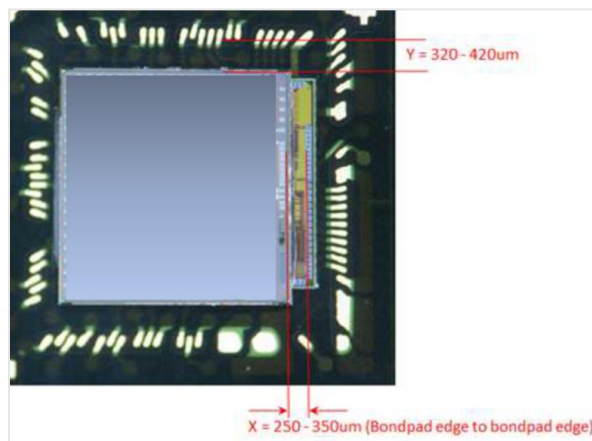


Fig. 4. Die placement requirement visual reference for BGA product

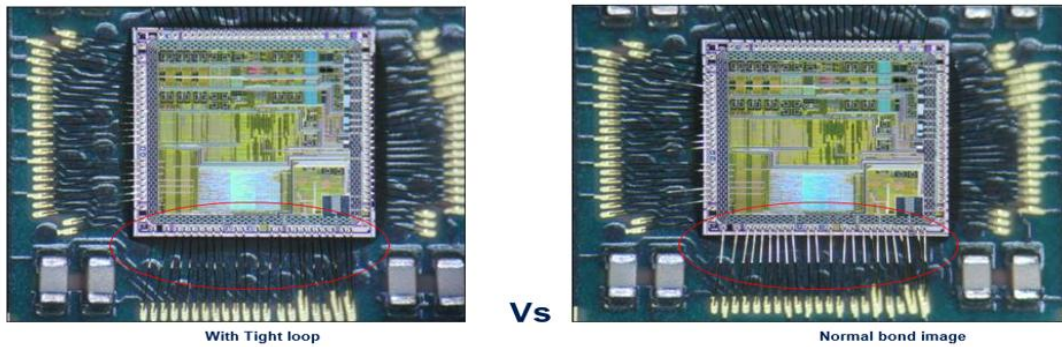


Fig. 5. Unit with tight wire loop versus units with normal/good loop

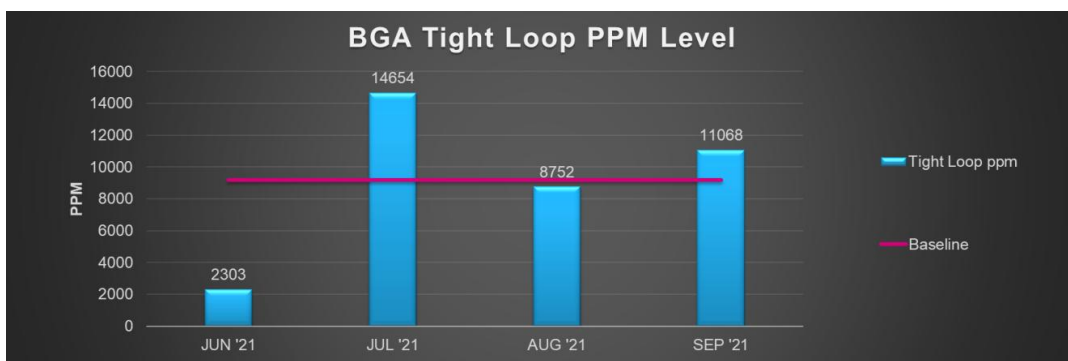


Fig. 6. BGA product history and performance

As specific die attach position is one of the passing requirements of the product, it also affects the output response and quality of wire bonded units. Die attach position or die placement defines the location of die for X and Y axis on the bond pad. Specific die clearance is pre-defined on development stage to ensure robust wire bond characteristic response. This includes wire loop, wire span, wire to die clearance and others. Parameters on die attach machine is set to have specific die placement with respect to machine capability and product's allowable tolerance. Fig. 4. Shows an example die placement requirement for both X and Y axis on BGA products that must be followed during machine set up and processing.

If this requirement is violated or unintentionally not followed due to certain reasons, it will affect the quality of the units specifically on Wirebond process. Rejections is expected and process yield will go down. One of these rejects is the Wirebond tight wire loop as seen on Fig. 5. To address the problem and its nature, history of lots and backtracking of product yield is considered. Fig. 6. Shows the product history and performance for 4 months including the production loading, and baseline for allowable reject in PPM (parts per million) level. This is

shown to identify the current condition, and how to respond with the problem. With this, a systematic approach will be used to have robust and quality corrective actions that will resolve the said phenomenon.

3. RESULTS AND DISCUSSIONS

To determine the root cause of the problem, input variables from the contributor process, which is the die attach, have been identified. Types and characteristics of these variables have also been enumerated, labeled as controllable or not, based on the detailed process flow of the said process as seen on Fig. 7.1. Three process steps were identified, and eight key process input variables, or KPIV's are determined as seen on Fig.7.2. From the 8 KPIV's, 3 of it were identified as critical based on the cause-and-effect matrix generated, as projected on Fig. 7.3. A Cause-and-Effect matrix shows process steps to input variables and correlates to process outputs variables of the said process. It connects key input variables to the key output variables such as customer's requirements using the process flow map as the primary source. These are the determining factor to generate a robust action and address the problem.

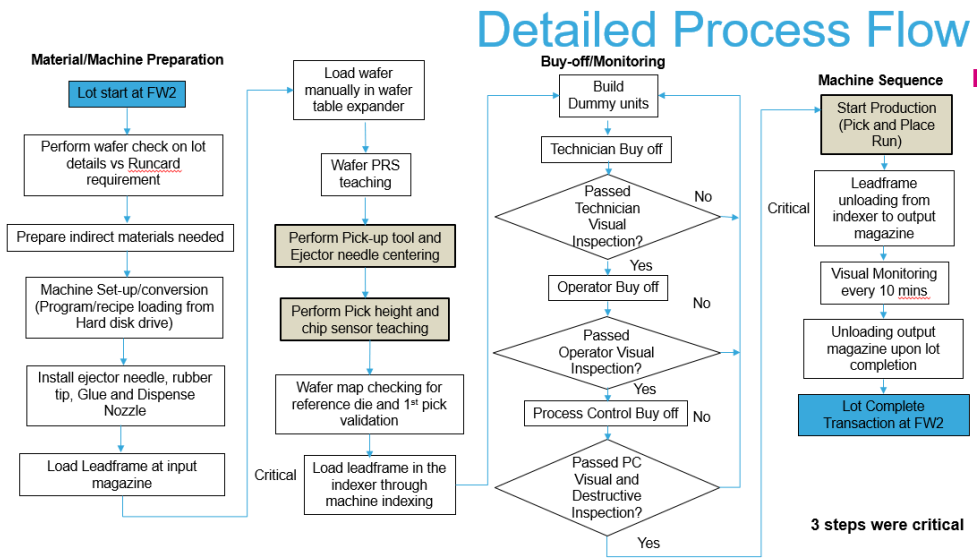


Fig. 7.1. Detailed Process flow of Die attach process

Process Inputs (KPIVs)				
Process Step	Type of Input	Input	Characteristic of Input (KPIV / X)	C/N
Perform Pick-up tool and Ejector needle centering	Raw Material / Information	Pick-up Tool	Type	Controllable
	Raw Material / Information	Pick-up Tool	Condition	Controllable
	Raw Material / Information	Needle	Type	Controllable
	Raw Material / Information	Needle	Condition	Controllable
	Human Resources	Technician	Knowledge	Controllable
Perform Pick height and chip sensor teaching	Human Resources	Technician	Knowledge	Controllable
Start Production (Pick and Place Run)	Equipment / Infrastructure	Bondhead	X-Placement Consistency	Controllable
	Equipment / Infrastructure	Bondhead	Y-Placement Consistency	Controllable

Fig. 7.2. Identification of Input Variables

Cause and Effect Matrix												
S.No	Process Step	Input	Characteristic of Input (KPIV / X)	Is Y Continuous / Discrete?		Total	Is X Continuous / Discrete?	Operating Range (for X)	Unit of Measure (UOM)	X Selected / Discarded?		
				Customer Priority	Discrete							
1	Perform Pick-up tool and Ejector needle centering	Pick-up Tool	Type	1	10	10	Discrete			0	0	Discard the X
		Pick-up Tool	Condition	1	10	10	Discrete			0	0	Discard the X
		Needle	Type	1	10	10	Discrete			0	0	Discard the X
		Needle	Condition	1	10	10	Discrete			0	0	Discard the X
		Technician	Knowledge	1	10	10	Discrete			0	0	Discard the X
2	Perform Pick height and chip sensor teaching	Technician	Knowledge	1	10	10	Discrete			0	0	Discard the X
3	Start Production (Pick and Place Run)	Bondhead	X-Placement Consistency	9	90	90	Continuous			0	1	Select the X
		Bondhead	Y-Placement Consistency	9	90	90	Continuous			0	1	Select the X

Fig. 7.3. Cause and Effect Matrix

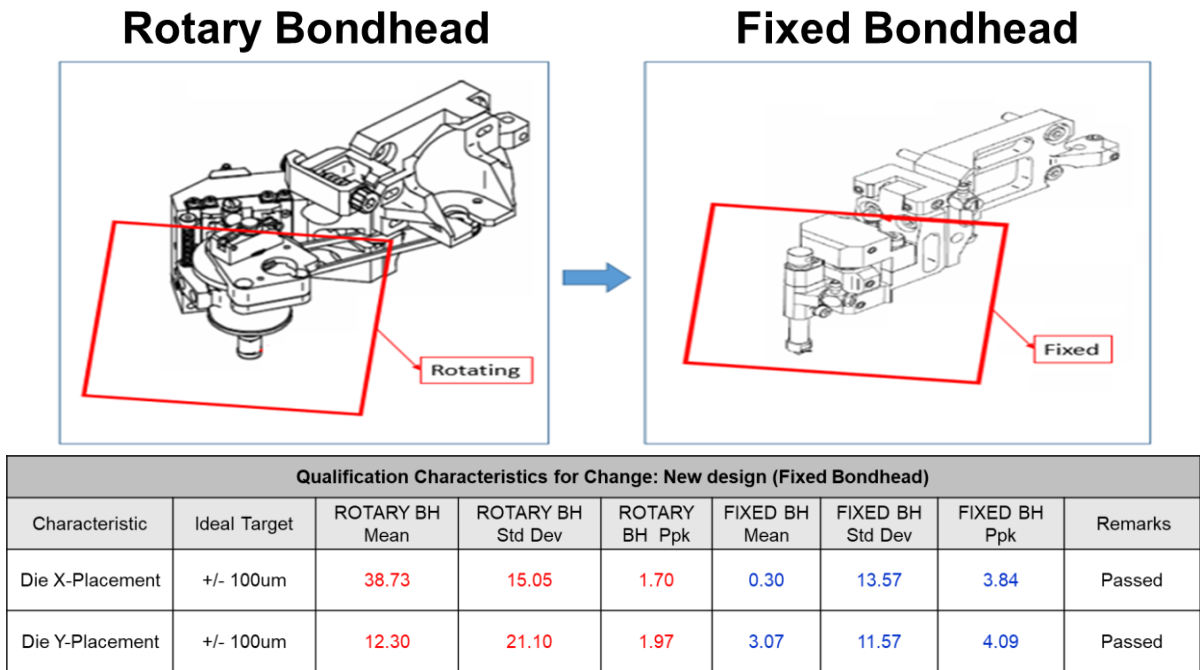


Fig. 8. Rotary bond head and Fixed bond head comparison

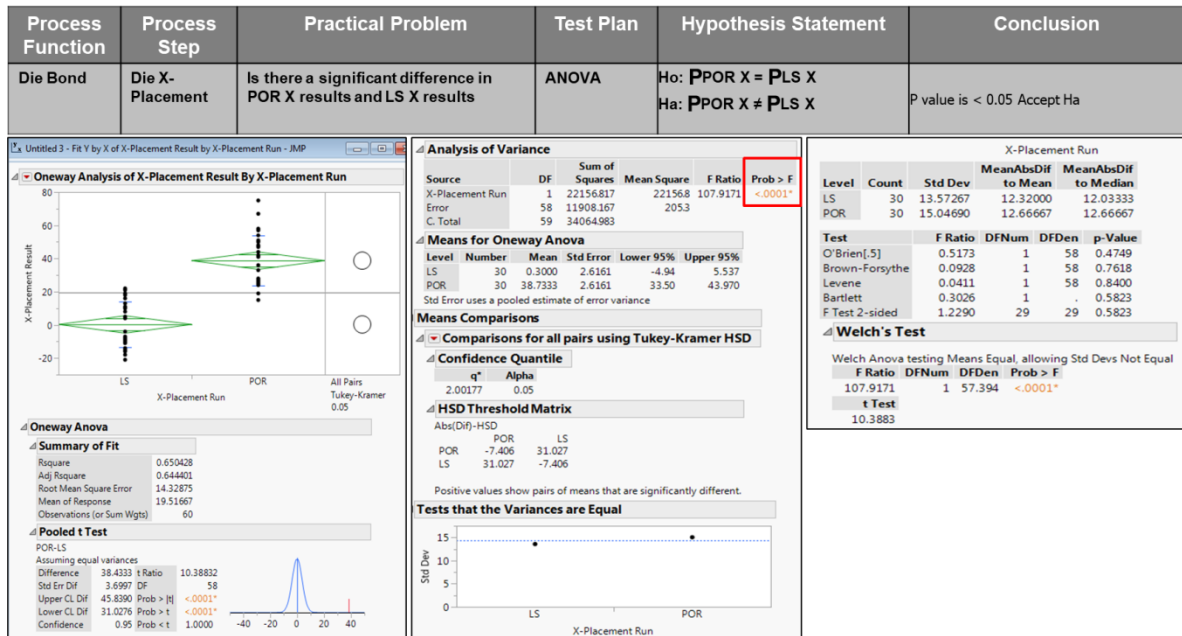


Fig. 9.1. Analysis of variance (ANOVA) for Rotary and Fixed Bond head for X-placement

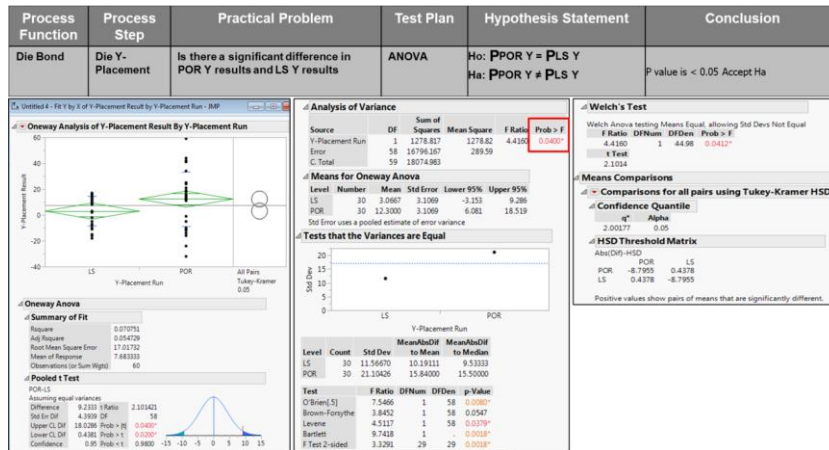


Fig. 9.2. Analysis of variance (ANOVA) for Rotary and Fixed Bond head for Y-placement

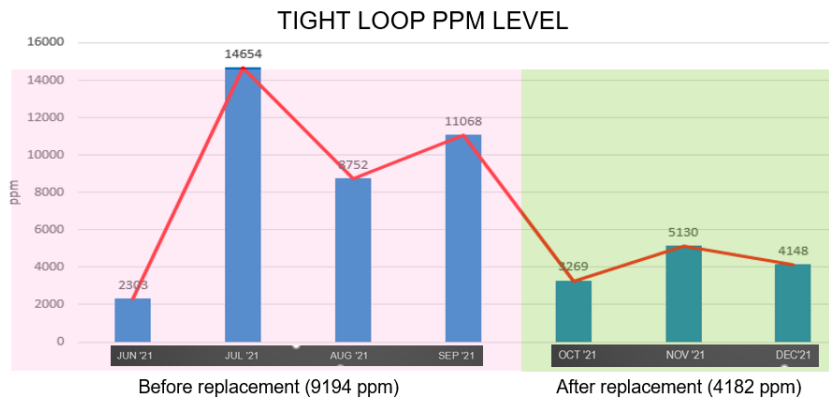


Fig. 10. Performance monitoring for tight wire loop defect

Die attach bond head performance and consistency is a big factor to have a robust die attach position or die placement as mentioned on the first part of the manuscript. The current design which is the rotary bond head provides acceptable results on die attach response and placement accuracy, but somehow produce units with tight wire loop on Wirebond process. This is because of the rotary design that exhibit rotation movement during die attach and affecting X and Y axis response of the units. To address the phenomenon, the team have introduced the Fixed design of the bond head. This is to prevent any unwanted movement of the bond head during die attach. Fig. 8 shows the comparison of the two designs and their construction. Statistical analysis was conducted to determine the effectiveness of the said action. As seen on Fig. 9.1 and 9.2 respectively, using Analysis of Variance or ANOVA test shows that there is significant difference between the rotary and fixed bond head responses on both X and Y placement having a P value of 0.0001 and

0.0400 respectively. It shows also that using fixed bond head does not only eliminate unwanted movement during die attach, but also improved the performance of die placement of units. Monitoring of processed lots after implementation also projected significant improvement on defects of wire bond process as shown on Fig 10, reducing the defect level of tight wire loop. With these results, it shows that using fixed bond head is better than the rotary one.

4. CONCLUSION AND RECOMMENDATIONS

In replacing the design of die attach machine from rotary to fixed bond head, robust and improved die placement is achieved and projected superb quality performance by means of maintaining desired position with accuracy. eliminating the moving part resulting to unwanted movements during die attach had resulted to a more robust process performance through

fundamental approach with the help of statistical analysis. It significantly improves the process yield and performance of the wire bond process with high defect levels of tight wire loop before the improvement. With this improvement on semiconductor manufacturing of BGA products, this is highly recommended to apply and fan out with the same or exact design of die attach machines provided with defined machine capability and product requirements. Continuous improvement is also noted to be considered to achieve desired performance on other semiconductor devices around the globe.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Rodriguez R, Gomez FR, Graycochea Jr. E. Die Placement Advancement for Prevention of Silhouetted Die Occurrence on LGA Package. Journal of Engineering Research and Reports. 2021;20(2): 113-117.
Available: <https://doi.org/10.9734/jerr/2021/v20i217270>
2. Liu DS, Chao YC, Wang CH. Study of Wire Bonding Looping Formation in the Electronic Packaging Process Using the Three Dimensional Finite Element Method. Finite Elements in Analysis and Design. 2004;40:263-286.
DOI:10.1016/S0168-874X(02)00226-3.
3. Chan YK, et al. Image based automatic defect inspection of substrate, die attach and wire bond in IC package process. International Journal of Advances in Science, Engineering and Technology. 2018;6(4),1: 53-59.
4. Rennier S, Rodriguez and Frederick Ray I. Gomez, A Study of Die Attach Process for Thin BGA Substrate Packages, International Research Journal of Advanced Engineering and Science. 2019;4(2): 86-90,.
5. Xu, Hui, Liu, Congzhi, Silberschmidt, Vadim, Chen, Zhong, Wei, J. The role of bonding duration in wire bond formation: A study of footprints of thermosonic gold wire on aluminum pad. Microelectronics International. 2010;27:11-16.
DOI:10.1108/13565361011009469.
6. Eng TC, et al. Methods to achieve zero human error in semiconductors manufacturing. 2006 IEEE 8th Electronics Packaging Technology Conference (EPTC). Singapore. 2006;678-683.
7. Pulido J, Rodriguez R, Gomez FR, Jr., EG. Mitigating Wire Short Defect on LGA Device through Substrate Design Optimization. Journal of Engineering Research and Reports. 2021;20(4):85-88.
Available: <https://doi.org/10.9734/jerr/2021/v20i417297>
8. Suboh MI, Ali MSS. Loop height assessment for automotive package,"2018 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC). 2018:500-505.
DOI: 10.23919/ICEP.2018.8374356.
9. Qin I, Milton B, Schulze G, Huynh C, Chylak B, N. Wong Wire Bonding Looping Solutions for Advanced High Pin Count Devices, 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016:614-621,
DOI: 10.1109/ECTC.2016.222.
10. Pulido J, Gomez FR. Enhanced wirebonding technique on qfn device with critical die reference. Journal of Engineering Research and Reports. 2021;20(3);57-61.
11. Moreno A, Jr, EG, Gomez FR. Wire Shorting Elimination through Wirebond Process Optimization of Semiconductor Sensor Device. Journal of Engineering Research and Reports. 2020;13(4):10-14.

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